EPSRC Mid-Range Facility for Group IV Epitaxy

1. Description of the Facility: (9000 char)

a brief description of the type of facility service proposed, and its function. An indication of what the facility should provide to be of maximum benefit to the research community and an estimate of the likely cost of the facility (for example, what size should it be, what technologies should it have available, how many staff would it need). All resource requirements should be clearly justified and prioritised in terms of "must have" and "desirable".

Recent consultation with the UK academic community and many years of collaborative projects demonstrate there is a healthy appetite for novel epitaxial Group IV semiconductor materials, devices and structures to be used across fields such as electronics, photonics, spintronics, energy, MEMS and quantum technology. The capability to deliver such epitaxy exists in the UK and could be effectively offered as a Mid-Range Facility (MRF).

Service Proposed:

A MRF for Group IV semiconductor epitaxy is proposed to supply bespoke wafers of epitaxial material containing layers of Si, Ge, Sn, C and their alloys to the academic community. The structures should include the option of grown-in n- and p-type doping profiles, thus placing the dopants where they are needed and avoiding damage from ion implantation. Both blanket and selective epitaxial growth; crystalline, polycrystalline and amorphous solid material; as well as low-dimensional structures (2D layers, 1D wires and 0D quantum dots) should be offered.

Users would be able to specify one-off designs, research batches with a range of parameter variations, or extended runs of over 100 identical wafers. The facility would include experts to discuss User requirements at the design stage, with a proper understanding of tolerances on each parameter to ensure the resulting material is both capable of satisfying the intended function and yet not over-engineered with the associated burden of cost and delays. A key feature of the service would include high quality materials characterisation to give Users important information not usually available with commercially obtained material.

The different lattice parameters of each Group IV element means strain can be introduced to epitaxial heterostructures. In some cases this is an important advantage for modifying material properties, in others it is an inconvenience to be overcome. Each layer within a heterostructure could be strained or relaxed and the characterisation performed should indicate this quantitatively.

Resource Requirements:

To deliver the service outlined above the facility would require:

(i) (**Must have**) Central to the facility is an industrially compatible, silicon-based, reduced pressure chemical vapour deposition (RP-CVD) system equipped with a range of precursor gases to enable matrix growth of Si, Ge, Sn, C and their alloys as well as dopant level introduction of elements such as B, As, and P. **Such a system can usefully produce ~1,000 research type wafers p.a. or over 10,000 production type ones.**
Cost using existing equipment is limited to maintenance and consumables of £170 k p.a. (see Justification)

If a new facility had to be set up the additional cost for system and installation of infrastructure would be ~£3.5 M (plus cost to build or adapt a cleanroom).

RP-CVD is the industry preferred epitaxy technique that, crucially, offers wafer-to-wafer reproducibility, uniformity across a wafer, and scalability by wafer size upto 450 mm diameter. To achieve this precision and reproducibility, each new design requires extensive calibration as the growth rate has a non-linear dependence on temperature, pressure and precursor gas flow rate.

Industrial RP-CVD installations are usually optimised to produce one structure only, with the growth recipes being sold by the equipment suppliers. By contrast this MRF would draw on epitaxy expertise already accrued from systematically optimising conditions for a wide variety of structures, using a range of precursors for different regimes, especially low temperature growth to supress segregation. Ultra-thin layers of highly strained Ge for high speed nanoelectronics, extremely clean thick Ge photonic detectors, 200 period Ge/SiGe MQWs with layer thickness controlled to <0.2 nm, and highly precise dopant control are examples that experts within the proposed MRF have already addressed.

The RP-CVD system offers capability to grow on 100 mm, 150 mm, or 200 mm diameter substrates. This range of sizes is important for compatibility with the various existing processing tools installed in academic labs across the UK. In addition, 100 mm pocket wafers would enable Users to grow on smaller 50 mm or 75 mm substrates, or other pieces of material. Substrates orientated along the standard (001) or alternative crystal directions could equally well be used to provide layers with different lattice parameters and properties. Growth on silicon-on-insulator (SOI), silicon-on-sapphire (SOS), GaAs and other wafers is also possible. In each case appropriate calibration would be performed.

(ii) (**Must have**) Solid-state molecular beam epitaxy (SS-MBE) is a technique very suited to research since parameters such as substrate temperature and growth rate can be independently adjusted (as opposed to RP-CVD where they are coupled). A Group IV MBE system is an essential part of the proposed facility to provide flexibility of response to User needs, be a second epitaxy source, and has its own specific advantages, e.g. very thin "delta-doped" layers can be deposited that prevent dopant atoms migrating within a structure. There is also greater flexibility to introduce new matrix or dopant elements through MBE: enabling new materials to be investigated; to grow isotopically pure Si and Ge epilayers; for in-situ thermal oxidation of Ge and Si surfaces to form high quality SiO_2 or GeO_2 dielectrics; or deposit multi-layered stacks of semiconductor-insulator-metal or semiconductor-magnetic materials with ultra-clean interfaces that are of huge interest and demand for new spintronic and electronic devices. The very wide growth temperature range from 20º C to 1000º C allows amorphous, polycrystalline or crystalline layers to be grown. The SS-MBE system would offer capability to grow ~200 wafers p.a. on 25 mm, 50 mm and 100 mm diameter substrates as well as on samples of arbitrary shape and size up to 100 mm. An optional upgrade would further enable growth on 150 mm and 200 mm diameter substrates.
Cost to run existing system ~£60 k p.a. + £90 k capital refurbishment of pumps.

Alternative purchase of new wafer scale Si-based MBE system would add a further ~£2 M.

(iii) (**Must have**) A distinctive feature of this facility would be to offer full material characterisation, including non-destructive mapping of the final delivered material as well as destructive testing of calibration wafers or segments of a divided final wafer. Key requirements for characterisation are access to rapid throughput and high-resolution x-ray diffraction, TEM, wafer scale optical imaging, AFM, spectroscopic ellipsometry, FTIR, photoluminescence, electrical characterisation by IV, CV and measurements of dopant distribution via SIMS.
Within the envisage delivery model new equipment to be sited alongside the epitaxy tools in the cleanroom would costs £750 k (XRD, SE, micro-PL, optical scan) with on-going costs to use these and to access existing state-of-the art TEM, HR-XRD and SIMS of ~£50k p.a.

(iv) (**Desirable**) There is increasing interest to produce epitaxy in limited area regions, either for control of strain during growth or in relation to the layout of devices on a circuit. A major issue in limited area epitaxy is in defining the areas for growth, usually by etching windows through an oxide mask, and ensuring the growth surface is perfectly clean. The facility to do this within the epitaxy cleanroom should be included, which means addition of a mask aligner, dry ICP etcher and oxidation furnace capable of handling full wafers.
Cost: £400k.

(v) (**Desirable**) The quantum technology and spintronics communities would like to work with isotopically pure materials, esp. 28Si, as 29Si is a spin impurity in natural Si. This can be delivered through MBE either by using an existing (large) SS-MBE system with capability to handle full wafers and a relatively large solid source of 28Si – cost £200k per source; or by assembling a dedicated small MBE system with a shorter source-substrate separation that can use a much smaller 28Si source. Cost system ~£250k, source ~£50k.

(vi) (**Must have**) Expert staff, who will ensure all Users get world class material on schedule that meets their original specification, are an essential part of the proposed facility. Epitaxy is a particularly specialised technique that just cannot be done on a DIY basis. The basic staff requirement is: two dedicated Senior Research Fellows, for growth and characterisation of materials by CVD and MBE, respectively; two technicians to support the infrastructure; an administrator to interact regularly with Users and ensure the MRF runs smoothly; partial allocation of senior academic staff to act as Director and provide expert advice. Staff Cost (**5.6 FTE**): £225 k p.a. + Indirects £140 k p.a.

TOTAL cost of running facility £0.65 M p.a. + initial costs £1.55 M. 5 year FEC £4.8 M. Excluding "desirable" facilities and assuming 80% funded the minimal 5-year cost to EPSRC could be £3 M.

2. Strategic Case: (9000 char)

an indication of which of EPSRC's strategic priorities are met by the research enabled by the proposed facility, and how these priorities would be met. A community perspective of the research enabled/supported by the proposed facility and the value added to existing research programmes and research priorities within the EPSRC theme that covers this remit. If the facility would enable cross-disciplinary research, please state here in which council's remit this would fall. An explanation of why this facility is now needed or will be needed in the future.

Group IV semiconductor materials have applications across the EPSRC Themes of *ICT*, *Energy*, *Engineering*, *Physical Science*, *Quantum Technologies* and *Manufacturing the Future*, as well as providing the silicon technology that underpins the whole of our electronic and data-driven society. Group IV epitaxy is a generic underpinning technique that is currently used by, and will become increasingly important for, researchers in many of the EPSRC supported areas including: *Optoelectronic Devices and Circuits*, *Optical Communications*, *Photonic Materials and Metamaterials*, *Materials for Energy Applications, Solar technology, Electrical Motors and Drives / Electromagnetics Microsystems, RF and Microwave Devices*, *Spintronics, Non-CMOS Device Technology, Sensors and Instrumentation*.

Silicon technology has driven the explosion in consumer electronic applications and has had a dramatic impact on our society and the world economy. The technology has advanced by continually reducing the size of transistors, whilst simultaneously increasing their switching speed and reducing power consumption. This has led to huge increases in memory density, processor capability, and commensurate reduction in cost per function. Today's silicon technology is probably the world's most efficient and highly optimised manufacturing industry. Many other technologies (e.g. those based on III-V semiconductors, graphene etc.) have been proposed to compete with silicon CMOS for logic applications, but none come close to delivering the same combination of performance, speed, integration density, and stability at a competitive manufacturing volume or cost. By developing novel structures that allow added functionality, Si technology is progressively moving into new applications, such as micro-systems, silicon-based photonics, spintronics, bioMEMS and even electronic refrigerators, all of which are set to benefit from the incredible integration that is achieved in Si electronics and the highly developed Si processing industry. As the range of applications broadens, increasing innovation is constantly required from the academic community and will undoubtedly produce step changes in the technology capability, provided that the community is suitably resourced.

Current and future Si technology would be better described as “silicon-based”; while starting from a Si or SOI substrate, the required functionality is realised by combining new structures and other Group IV materials such as Ge, Sn or their alloys with Si. Such layers (and hence the advanced devices) can only be made with the atomic control of epitaxial growth. Specifically, Ge has already been shown to be a viable high speed electronic material; creation of the necessary strain in the Ge or addition of Sn provides opportunities to create truly direct band gap material and thus remove the one disadvantage that Group IV materials have compared to III-Vs.

The specific requirements for Group IV epitaxy can be categorised into several areas:

(a) Integration with silicon – there is strong motivation to integrate all manner of devices and sensors with silicon electronics and for mounting on a common platform, which by default is a Si(001) substrate, leading to system on a chip solutions. The Group IV Epitaxy Facility would supply buffer layers of $Si_{1-x}Ge_x$, Ge or $Ge_{1-x}Sn_x$ on Si to enable lattice matching of subsequent III-V, or other, materials. These buffers would be smooth, fully-relaxed and with a lower defect count than could be obtained anywhere else in the world. The demand for integrating direct bandgap III–V components, with their robust photonic properties, on Si was clearly evident from the III-V Technologies community meeting held recently in Birmingham and could provide a route for future photonics.

(b) Group IV devices – rather than using the silicon-based epitaxy as a support for other technologies, devices and sensors can be built from the Group IV materials. Motivation for this is driven by the need for cost effective consumer devices based on abundant resources and energy efficient manufacturing. A prime example is the field of Si Photonics where signal encoding, multiplexing, transmission, de-multiplexing and detection can all be achieved with Group IV materials. Research effort is still required to find an effective Group IV source, but recent advances with strained Ge and $Ge_{1-x}Sn_x$ point towards creating a direct bandgap material. Si photonic circuits underpin a tremendous range of applications in quantum computing, quantum simulations, quantum communications, quantum sensing, atomic clocks & positioning systems. Similarly, Group IV devices can be used for detection across the electromagnetic spectrum and especially in the infrared/THz range for healthcare, security, and gas sensing, along with fast integrated switches for data-centres and fibre-to-the-home. Such activity is key to the ICT priority theme of ‘*Photonics for Future Systems*’.
The diversification of applications for Group IV semiconductors is reflected in EPSRC’s strategy to refocus activity from CMOS Device Technology, which it considers to be a mature technology (notwithstanding the enormous global effort by semiconductor companies to continue improvements) into the wide range of *Non-CMOS Device Technology* and activity that is termed ‘*Beyond-CMOS*’ and ‘*More-than-Moore’*. Whereas CMOS devices can be made directly on bulk silicon wafers, the new devices increasingly require epitaxy and introduction of other Group IV elements. Having a dedicated UK Group IV epitaxy facility would enable more UK researchers to move into this burgeoning field.

(c) Quantum Technology – realisation of the UK’s ninth Great Technology relies on efficient single photon propagation, manipulation and detection. Low-loss quantum photonic circuits can be built from Group IV waveguide and utilise, for instance, fully-integrated Ge-on-Si single photon avalanche diodes (SPADs) produced epitaxially for photon detection at λ~1550nm. Other implementations of quantum devices rely on interaction with single spins in a material such as silicon or diamond. Again the high purity obtained with Group IV epitaxy is essential and may involve growth from isotopically pure sources. Quantum information processing (QIP) devices can be built around quantum dots that would be supplied through epitaxy. For ultimate sensitivity operation at very low temperature is required to reduce noise: electronic cooling based on Group IV tunnel junctions is being explored in this area. In the long term, research into high mobility

spintronic systems will lead to new quantum and spintronic technologies. In the short term, there is strong interest from a pure research perspective in coherent and interaction based phenomena in low-dimensional electron and hole systems with the high mobility now being obtained in Ge.

(d) Micromechanical devices – the ability to create heterostructures of different Group IV materials that can be etched selectively presents opportunities for creation of MEMS/NEMS structures, such as membranes, wires and tubes. By also selectively doping these layers the electronic and/or optical properties of the resulting structures can also be controlled. The facility would provide both the structures required and expert advice on the best approach to processing.

(e) Energy Harvesting – many different routes to energy harvesting rely on Group IV materials: the MEMS structures described above can act as micro-mechanical energy harvesters; SiGe based thermoelectric devices are used at high temperature for energy generation in satellites and could be engineered for efficient room temperature operation; Ge layers are already incorporated with III-Vs in multi-junction solar cells and the addition of Sn expands the accessible bandgaps opening the possibility for efficient, all Group IV multi-junction cells and for high temperature energy harvesting via thermophotovoltaics. There is also still a lot of research activity on crystalline, polycrystalline and amorphous Si for photovoltaic applications where epitaxy can lead to improved performance and even reduce costs.

(f) Power electronics –in 2011 BIS published '*Power Electronics: A Strategy for Success*' which identified this as a priority area for the UK. Currently, the majority of power electronic devices are made from Si and operate at < 1 kV. For higher voltages, a major requirement is to have a thicker layer of semiconductor that can be doped (by epitaxy rather than implantation) to sculpt the electric field and is defect free to prevent breakdown. The proposed facility could supply Si epitaxial layers thicker than the current standard of 30 um with a quality exceeding that available commercially and enabling Si devices to operate at higher voltages. Future development of SiC epitaxy is also envisaged (Section 6).

3. Impact: (4500 char)

A description of the impact the proposed facility would have on the research community, across the range of types of impact (scientific/academic, people, economic, skills and training, socio-economic etc.).

Devices that incorporate Group IV epitaxy can have a major impact across economic sectors from aerospace to healthcare. Compatibility with silicon provides huge advantages in the ability to interface novel devices with "standard" Si electronics and Si photonics, and especially where marketable devices are concerned to benefit from the optimised mass production capability. In this framework economic impact can quickly follow scientific demonstration, either through investigator led spin-outs or technology licensing. A key feature for the Group IV community is the availability of centralised processing expertise, such as the James Watt Nanotechnology Centre in Glasgow with its pipeline to commercialisation through Kelvin Nanotechnology, the Southampton Si Photonics facility with connections to companies such as Oclaro, as well as the scale-up route for epitaxy through IQE Silicon.

The community was asked to highlight areas of scientific and economic impact that would follow from developments in Group IV epitaxy and some examples are given below:

- High speed and bandwidth single chip photonic solutions for data centres and fibre-to-the-home achieved by integration of Ge and SiGe active devices into Si photonics platform technology.
- Silicon based light sources are very difficult to realise, but a silicon light source of even reasonably efficiency would revolutionise both data communications and optical sensing.
- Achieving fast, low-noise single-photon detection, ultimately in a waveguide configuration for integration with sensing and quantum circuitry. Arrayed detector operation is another exciting avenue of research. Maximum impact will be via using Peltier-cooled semiconductor-based SPDs

rather than low-temperature superconducting detectors. Potentially useful in quantum sensing, quantum communications, quantum imaging and quantum processing applications.

- Cheap and high pixel density thermal imaging cameras using 2D arrays of Ge SPADs operating at room temperature for 1.3 and 1.55 micron wavelengths with single photon sensitivity for healthcare, security and defence applications
- Complete mid-infrared sensing technology on a silicon platform to deliver a cheap sensing technology for security, healthcare and environmental sensing applications.
- Reduced CO_2 emission through autonomous sensors powered by heat and recovering over 5% of the automotive fuel waste that goes down an exhaust pipe in all vehicles, delivered via high efficiency Si-based thermoelectrics.
- Tunnel FETs with high on-current and < 62 mV/dec sub threshold slopes used in CMOS processes for high-density, low-power microelectronics.
- A single chip MEMS gradiometer with integrated laser interferometer to allow the military to see through walls and for civil engineers to dig holes in the correct places to service utilities (3 out of 5 holes are in the wrong place costing the UK £2.2 B p.a.) and for oil companies to improve prospecting through geological mapping.
- Integration of III-V's on silicon for low cost higher bandwidth communication systems.
- Higher efficiency concentrator PV technology.
- Both thermometry and quantum information processing (QIP) applications require very low charge noise and low electrostatic disorder, for which undoped Si/SiGe quantum wells seem very suitable. Thermometry advances (plus new electronic refrigeration techniques) could enable nanoelectronic devices to be studied in a new temperature regime below 1 mK. Improvements in Si/SiGe quantum dot reproducibility and stability would improve the potential for scaling up Si-based QIP devices.
- Building a quantum computer and/or quantum sensors based on Group IV nanostructures that outperform classical devices; improved fundamental understanding of the quantum to classical transition. Unique properties of novel 2D materials such as graphene-, silicene-, germanene, stanene could lead to a new generation of quantum devices, where quantum coherence, entanglement and superposition are established and maintained.
- Spin injection/manipulation/detection in Si and Ge, spin amplification, topological insulator spintronics and thermoelectrics, epitaxial combination of dissimilar materials for new functionalities, leading to energy-efficient computing etc.

4. Users: (4500 char)

A description of who will benefit from the existence of this facility, including the number and type of researchers (both academic and industrial) in the UK who are likely to want to use it. Information should be provided on the likely main users, where they will be based, and projected growth in the user base over the next 5 years. Where appropriate, please indicate the need for remote access and any other specific access requirements in order for the research community to get optimal benefits from the facility.

Current and previous collaborators who have benefited from joint research on UK grown Si-based epitaxial material include academics from twenty UK universities: Birmingham, Cambridge, Cardiff, Exeter, Glasgow, Heriot Watt, Imperial, Leeds, Liverpool, Manchester, Newcastle, Oxford, RHUL, Sheffield, Southampton, St Andrews, Surrey, UCL, Warwick, York.

This set of UK universities provides an essential user-base of over 100 currently active academics together with their post-doctoral researchers and graduate students. Of these, 22 senior academics who lead their own groups would be potential major Users and have contributed to this Statement of Need, as listed in Section 8. *The timescale and limited resources available to prepare this document meant that not all potential users have contributed directly, but can nevertheless be expected to utilise the facility once established. We can explicitly identify a further 25 permanent UK academics who would be* potential Users and, in addition, we expect more academics from the III-V materials/devices

and Si power electronics communities to become new Users of the facilities. As more researchers become aware of easy access to highly specified Group IV epitaxy, and the range of applications for which it is recognised as competitive grows, we can confidently expect the user-base to double over the next five years.

An annual User Meeting would be held that will spread knowledge amongst the community. Users will learn of the range of projects supported, latest developments in Group IV epitaxy and devices, and community networking could generate novel ideas and proposals for future development of the facility. These meetings will be publicised beyond existing Users to involve the wider academic and industrial communities and act as showcase for what can be done with Group IV epitaxial materials.

Epitaxy produced in the UK has also been instrumental in research collaborations with international centres of excellence such as IMEC (Belgium), CEA-LETI, CNRS-Minatec (France), Jülich (Germany), VTT (Finland) and international universities of UCL (Belgium), Aalto (Finland), Politechnique Milano, Bologna, Pisa (Italy), Aachen, Stuttgart (Germany), ITE (Poland), ICN Barcelona (Spain), KTH, Chalmers (Sweden), ETH Zurich (Switzerland), Tokyo, Kyoto, Tohoku, Yamanashi, Keio (Japan), MIT (USA). Material could be supplied to international partners either within the framework of internationally funded projects or with an appropriate cost model for direct access. One example of this is the recently submitted H2020 action driven by the SiNANO Institute *Nanoelectronics for the New Era* (NE2) that proposes a model for international access to facilities based on unit costs. Glasgow, Liverpool, Newcastle and Warwick are all active members of SinANO that encourages pan-European collaboration in the field of microelectronics and More-than-Moore activities.

In addition, the academic staff associated with the facility will maintain an international profile and bring major meetings to the UK e.g. International Conference on SiGe Materials and Related Devices, which will be self-supporting and not require funding from the facility.

5. Justification (4500 char)

An explanation of why the mid-range facility model is the most appropriate, as opposed to other approaches (such as local provision / strategic equipment, etc.). Reasons to be considered may include the need for specialised expertise in the technique, a new technique that is still at the early stages, unique capabilities (rather than just extra capacity), efficiencies of scale, fostering new communities or any other well founded and clearly explained justifications for a Mid-range Facility.

The current state of Group IV epitaxy technology delivered by RP-CVD is such that a facility can offer a wide variety of simple or complex structures. The reproducibility of the technique means it can reliably repeat designs over many wafers and over an extended period of time, unlike previously when supply was primarily based on MBE. Hence, sufficient material can now be readily supplied to Users who want to engage in complex device fabrication research and/or development of novel device prototypes, where many identical development wafers are needed to tune the processes.

The operational model would be for Users to contact the facility with their requirements, discuss technical details and iterate to an acceptable specification that would be grown, with characterisation as required, by the facility staff. The specific and demanding technical requirements of epitaxy mean that it is far more efficient for dedicated experts to perform the growth than for Users to do this themselves.

The alternative of individual groups setting up their own epitaxy systems would be prohibitively expensive and not efficient compared to the facility model, given the infrastructure and expertise required. Furthermore, the potential throughput of the systems that would be part of the MRF would be sufficient to satisfy the expected needs of the relevant community for research investigations. Expanding activity to commercialisation levels would require additional epitaxy systems that could be

purchased through the facility, but would most likely be better served by partnership with commercial services.

A major issue with running complex epitaxy facilities is the need to repair systems quickly without having to wait for approval of funding. Within the facility model a minimal set of spares can be held on site and a reserve fund will be retained to cope with unexpected failure. By comparison, it is incredibly difficult to support epitaxy facilities based on intermittent funding from individual projects that neither guarantee continuity of expert staff or of equipment maintenance.

Over the past 6 years, Warwick has produced some 500 wafers each year by RP-CVD, demonstrating the MRF can deliver. This costs £150k p.a. for consumables such as: ultra-high purity carrier and purge gasses; matrix and dopant precursor gases; gas panels, purifiers, detectors; Si wafers, storage and shipping trays; wet chemicals for cleaning prior to growth; safety related clean room (ISO 3 -6) consumables; and £20k p.a. for essential spare parts. For reference, an annual service contract with the RP-CVD manufacturer would instead be ~£150k, with spare parts extra.

The experience of the community is that Users want to control their own processing routes independently of the material growth. Facilities to process Group IV materials exist in many individual labs in addition to EPSRC supported central facilities, particularly those in Glasgow and Southampton which could work very closely with this proposed MRF.

We should note at this point that the outcome of consultation with the potential User community for Group IV semiconductor materials was a majority view in favour of establishing a separate entity to the existing EPSRC Mid-Range Facility for III-V Technologies – a view shared by that facility. Despite both facilities performing epitaxy the materials systems are distinct, with different systems and consumable demands, the user communities of a different scale and the proposed access models sufficiently different. There would be little if any economy of scale in combining the two activities and only a further level of administration introduced. Nevertheless the two facilities could enjoy a healthy coexistence, in particular collaborating by the Group IV facility supplying lattice-tuned buffer layers for integration of III-Vs on Si.

Comments from the community include:

> "It is important that the community is able to access high quality structures without needing to go through the process of a full EPSRC grant review. I would like to see a generous provision of pump-priming wafers to try out new ideas."
>
> "I would prefer to see III-V and group IV growth kept separate. A smaller facility with more personal contact and the possibility for writing joint grant applications suits me much better than a large national facility."
>
> "I think Si and III-V are rather different, they serve different communities, have different challenges and require different expertise."

6. Sustainability (4500 char)

Please describe how the facility would ensure its future sustainability. Outline a suitable access model and justify access provided free at the point of use for a particular access type or special user groups (e.g. pump priming access, access for students, new capabilities, …) Please give an indication of other possible sources of financial support and the potential for recouping costs through charging.

Access model:

The highest priority for the Group IV epitaxy facility is to offer fast turn-around from conception of ideas to delivery of epitaxy on the scale of a few weeks to a few months. This activity is expected to represent 40% of the time available in the growth systems. For "standard" growth requests of a few wafers this would not require the User to provide any funding in addition to the EPSRC support

received for the facility. This type of activity is seen as particularly suited to supporting early career academics and for trial of truly novel ideas that might not be supported by the peer review process. In cases where particular non-standard substrates or exotic precursors would be required, Users would be requested to cover the additional direct costs incurred.

20% of activity would be for larger projects, which can take a number of forms. User requests for multiple or similar copies of a particular design will be fulfilled on the basis of Users contributing to the materials cost, with facility staff and time being already funded via the EPSRC facility support. Very complex designs that require extensive process development e.g. quantum cascade laser structures of several thousand epilayers, could be undertaken but would require further project based grant support to provide the additional consumables and additional dedicated staff to complete the characterisation associated with prolonged process development, although the individual project grant would still avoid the cost of the underpinning infrastructure provided through the facility agreement. Should demand for this element outstrip the facility's capacity to supply then additional staff would be appointed to the MRF. Ultimately, it would be scalable through purchase of additional machines if the 10,000 wafer p.a. limit was exceeded.

20% of machine time would be reserved for maintenance and internal calibration activity to ensure the facility is kept in reliable working condition over the longer term.

The final 20% of system capacity would remain outside of the MRF and by reserved for research by facility staff to develop novel epitaxy techniques, new material combinations, and thereby stay at the leading-edge of the field in order to ensure the service offered to Users remains state-of-the-art internationally. Funding for this activity would be from separate research grants.

Allocation of time on the facility would be made by the local administrator under guidance of the facility Director and a MRF management group consisting of academics from a range of institutions.

Facility Development

The sustainability of the facility will principally be ensured by establishing and maintaining a highly satisfied user base who recognise that they are receiving world class material delivered to schedule. The facility would guarantee to be an on-going source of material to the community, and to develop new materials of interest e.g. Si-Ge-Sn-C.

Provided that this overarching principle is followed the financial sustainability of the facility will be ensured by User demand and by funded projects that emerge from the pump priming activities. Greater access to Group IV epitaxy from a wider community will lead to further ideas and developments. Facility academics will work with UK academic Users to propose new projects for funding via Research Councils, H2020 and elsewhere. Good contact with European networks of universities e.g. SiNANO, will help leverage European funding for the UK.

Scale-up of successful research outcomes from the facility, e.g. via IQE Silicon or university spin-outs, will generate additional employment and economic impact in the UK and consequently redirect further support to the academic community. Such transfers of intellectual property would be via a license agreement and/or consultancy which would generate additional income to support the facility.

Furthermore, the facility could be developed to include SiC epitaxy for >10 kV devices using the dedicated SiC RP-CVD facility recently purchased by EPSRC and installed in Warwick as the only such system in the UK. This system is currently in its commissioning phase. After about a year of research activity we expect sufficiently robust growth processes to have been developed for these to be incorporated in the MRF to serve the UK power electronics community.

7. Context (4500 char)

What facilities of this type already exist (a) at the university level, (b) at the national or regional level and (c) at the international level? How accessible are these existing facilities to UK academics? An explanation of how the proposed facility will compliment or enhance local, regional and/or national research capability. If EPSRC was unable to support this facility, what would the research community do? (for example, in terms of seeking access to non-UK facilities).

Within UK academia there is currently only one facility, at Warwick, that can deliver Si-based epitaxy at wafer scale and in large quantities. It consists of RP-CVD and SS-MBE tools which have, to now, been supported on individual project grants. Wafers have been made available to UK academics via funded collaborative projects on which Warwick have been partners e.g. '*UK Silicon Photonics*', '*Renaissance Ge*', '*Silicon Resonant Tunnelling Diodes and Circuits*', as well as small numbers of wafers supplied as unfunded pump priming activity. UCL recently invested £2 M to connect a 3" GeSiSn MBE reactor to their III-V MBE reactor, specifically to investigate monolithic integration of III-Vs with Si, which should be running by summer-2015. Within the proposed MRF model it will be possible to respond much more rapidly to research ideas, within a matter of weeks rather than at least a year required between conception and funding for a typical grant; prevent the large overhead costs of running a facility from distorting the cost of individual projects; and establish the supply of *ad hoc* wafers on a financially sustainable basis. By removing the barrier of obtaining a fully funded research grant, academics will more easily be able to try out new ideas and be competitive globally in this fast moving field.

The provision for Group IV semiconductors within the UK contrasts markedly with that for III-V materials where there is already a *Mid-Range Facility for III-V Technologies* and additional capacity within many universities that have their own III-V epitaxy systems. If the current Group IV systems were lost there would be no UK academic source of Si-based epitaxy.

At the national level, it is possible to purchase Si or Ge epitaxy, in practice just from IQE Silicon in Cardiff, but only for a very limited set of designs, without characterisation of the material actually supplied, and usually only in bulk quantity. The proposed facility would be capable of supplying single (or multiple) wafers of custom design agreed with the User. Crucially, the facility would include full material characterisation, enabling appropriate batch splits to be designed and evaluated for research. All designs would be retained and the reproducibility of RP-CVD means that accurate repeats could easily be supplied either singly or in volume well beyond 100's of wafers. For standard structures the cost per wafer would then be relatively low e.g. < £250 per wafer. If significant volume was required e.g. for pre-production trials in a spin-out, then the designs could be directly exported to IQE under license for mass production, since the same growth recipes are used in the academic and commercial systems.

At the international level, Si-based epitaxy can be obtained from large research facilities in Europe (IMEC, LETI, KTH, Fraunhofer IZM, FZ Jülich) at a cost (often several €10,000's per simple structure as a minimum) and with limited flexibility. Similar, facilities and companies exist in USA and Japan. Various Chinese institutions offer material for sale, but the quality is extremely variable and

unpredictable. However, many companies and research centres have recently upgraded their entire tool set to use 300 mm diameter wafers as the standard size for epitaxy and device fabrication. Until this happened, very productive joint collaborative projects were possible on SiGe and Ge epitaxy with both LETI and IMEC (e.g. EPSRC *Renaissance Ge*), but due to this wafer size restriction it is now virtually impossible for university research groups to collaborate with them. This is another key reason why the UK should have an independent facility to offer flexibility in providing epitaxial materials on wafers with diameters below 200 mm that can be handled by the existing tool sets in UK universities. In due course we could expect such material to also be in demand from university groups in other countries.

UK academics have obtained material via collaboration with von Känel's group at PoliMilano, but this is produced by a plasma enhanced CVD technique that has inherent composition and thickness variation of up to 200% across a 4" wafer. Research collaboration with other groups worldwide is of course possible through personal contacts, but is especially hard for early career academics to establish. The lack of a dedicated UK Si-based epitaxy capability would restrict the UK to be followers rather than leaders in this field and effectively preclude economic impact.

8. People (4500 char)

A list of who was involved in preparing this statement of need (name, institution and research interests).

The following academics have been involved in preparing this Statement of Need:

Prof Tim Ashley [University of Warwick] Group IV substrates for III-V devices in areas including low power electronics; spin-based devices; infrared sources and detectors; magnetic field sensors

Dr Crispin Barnes [University of Cambridge] Spintronics, Quantum technology

Dr Gavin Bell [University of Warwick] Spintronics, Thermoelectrics

Prof. Gerald Buller [Heriot-Watt University] Photonics (detectors), Quantum technology

Prof. John David [University of Sheffield] Photovoltaics, Photonics (detectors)

Dr Liam O'Faolain [University of St Andrews] Photonics (sources, other)

Dr Frederic Gardes [University of Southampton] CMOS Integrated photonics and Electronics

Dr C.H. "Kees" de Groot [University of Southampton] Nanoelectronics

Dr Zoran Ikonic [University of Leeds] Photonics (sources, detectors, other), Quantum Technology, Electronics, Photovoltaics

Prof. Thomas F Krauss [University of York] Photovoltaics, Photonics (other)

Prof. David Leadley [University of Warwick] Electronics (logic, power), Spintronics, Photonics (detectors, sources, other), Quantum technology, Thermoelectrics, MEMS

Prof. Huiyun Liu [University College London] Photovoltaics, Photonics (detectors, sources, other), Quantum technology, Thermoelectrics

Dr Goran Mashanovich [University of Southampton] Mid infrared photonics (Passive, Detectors, Modulators)

Dr Gavin Morley [University of Warwick] Spintronics, Quantum technology

Dr Maksym Myronov [University of Warwick] Electronics (logic, power), Spintronics, Photovoltaics, Photonics (detectors, sources, other), Quantum technology, Thermoelectrics, MEMS

Prof Anthony O'Neill [Newcastle University] nanoelectronics, ferroelectrics, power electronics, energy harvesting, Si nanowires, heterogeneous integration

Prof. Douglas Paul [University of Glasgow] Electronics (logic, memory, rf, power), Spintronics, Photovoltaics, Photonics (detectors, sources, other), Quantum technology, Thermoelectrics, MEMS

Prof. Sir Michael Pepper [University College London] Electronics, Quantum technology,

Dr Jonathan Prance [Lancaster University] Quantum technology

Prof. Graham Reed [University of Southampton] Si photonics (Detectors, Modulators)

Prof Alwyn Seeds [University College London] Photonics devices, integration of III-V photonics on Si substrates

Dr Thomas Walther [University of Sheffield] Electronics (memory), Spintronics, Photovoltaics, Photonics (detectors, sources, other), Quantum technology